REMARKS/ARGUMENTS

The Office Action mailed June 20, 2003, has been received and reviewed. Claims 1 through 6, 9 through 24, and 27 through 32 are currently pending in the application. Claims 2, 11 through 18, and 20 have been previously withdrawn from consideration as being drawn to a non-elected invention. Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, 28, and 30 through 32 stand rejected. The Office Action Summary states that claim 29 also stands rejected; however, the body of the Office Action does not state a basis for such rejection. Claims 3 and 21 have been amended, and claims 1, 2, and 11 through 20 have been cancelled herein. Applicant respectfully requests reconsideration of the application in light of the above amendments and the following remarks.

Amendments to the Specification

Paragraphs **[0002]**, **[0056]** and **[0061]** have been amended herein to correct minor editorial problems. It is respectfully submitted that the amendments are supported by the as-filed specification and drawings and no new matter has been added.

35 U.S.C. § 103(a) Obviousness Rejections

A) Applicable Authority

The basic requirements of a *prima facie* case of obviousness are summarized in MPEP §2143 through §2143.03. In order "[t]o establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings. Second, there must be a reasonable expectation of success [in combining the references]. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." Further, in establishing a *prima facie* case of obviousness, the initial burden is placed on the

Examiner. "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985). *See also* MPEP §706.02(j) and §2142.

B) Obviousness Rejection Based on U.S. Patent 6,124,189 to Watanabe et al. in View of U.S. Patent 6,479,899 to Fukuda et al.

Claims 1, 3 through 6, 9, 10, 19, 21 through 24, 27, 28, and 30 through 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,124,189 to Watanabe et al. (hereinafter the "Watanabe reference") in view of U.S. Patent 6,479,899 to Fukuda et al. (hereinafter the "Fukuda reference"). Claims 1 and 19 have been cancelled by way of the present communication and, thus, it is respectfully submitted that the rejection as to these claims has been rendered moot. As the Examiner has failed to establish a *prima facie* case of obviousness of claims 3 through 6, 9, 10, 21 through 24, 27, 28, and 30 through 32 based upon the Watanabe reference in view of the Fukuda reference, Applicant respectfully traverses this rejection, as hereinafter set forth.

Referring initially to claim 3, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest all of the limitations recited in this claim. Independent claim 3, as amended herein, recites a transistor for dissipation of electrostatic discharges. The transistor comprises, in part, an intermediate structure comprising a substrate having at least one thick field oxide area and at least one active area including at least one implanted drain region and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The transistor further comprises a first barrier layer planarized down to the at least one transistor gate member and substantially covering the at least one thick field oxide area, the at least one active

area and adjacent the at least one transistor gate member. Still further, the transistor of independent claim 3 comprises at least one drain contact plug and at least one source contact plug, both extending through the first barrier layer, and in electrical communication with the at least one drain region and the at least one source region, respectively, on the semiconductor substrate. The transistor further comprises an individual drain contact land disposed atop each of the at least one drain contact plugs and a portion of the first barrier layer and an individual source contact land disposed atop each of the at least one source contact plugs and a portion of the first barrier layer. The individual drain contact land is wider than the at least one drain contact plug and the individual source contact land is wider than the at least one source contact plug. A second barrier layer is disposed over the first barrier layer, the individual drain contact land and the individual source contact land. *At least one upper source contact extends through the second barrier layer, the at least one upper source contact being in electrical communication with at least one of the individual source contact lands, and at least one upper drain contact extends through the second barrier layer, the at least one upper drain contact being in electrical communication with at least one of the individual drain contact lands.*

The Watanabe reference, on the other hand, discloses a metal strapped polysilicon gate metallization structure for a semiconductor device and method of forming the same. *See, Watanabe reference* at Abstract; col. 2, lines 18-20. The metal strapped polysilicon gate structure of the Watanabe reference includes a p-type silicon substrate 100 having an active area which is isolated from other elements by shallow trench isolation regions 101. Spaced apart source/drain diffusion regions 107 are formed in the substrate and a gate structure 130 is insulatively spaced from a channel region between the source/drain regions 107 by a gate dielectric film 102. *See id.* at col. 3, lines 37-55. An insulating layer 108 is formed on the silicon substrate 100, the shallow trench isolation regions 101 and the source/drain regions 107. *See id.* at FIG. 7B; col. 5, line 65 – col. 6, line 10. Contact openings 109 are formed in the insulating layer 108 and include a titanium/titanium nitride layer 110 on the sidewalls thereof. *See id.* at col. 6, lines 9-12. The contact openings 109 are filled with a conductive material layer 111C. A second insulating layer 112 is formed over the first insulating layer 108 and openings

113 are formed therein. The openings are filled with a conductive material to form wiring layer 114. *See id.* at FIG. 7B; col. 6, lines 15-20.

Applicant submits that, contrary to the assertion at page 2, ¶5 of the outstanding Office Action, the wiring layer 114 of the Watanabe reference is not a contact land as claimed in each of independent claims 3 and 21. Instead, the wiring layer 114 is similar to the source contact metallization 252 and drain contact metallization 254 as described in the present application with reference to the prior art. *See, Specification*, ¶ **[0007]** and FIG. 38. Even if the wiring layer 114 may be used to form multilevel structures, as asserted in the outstanding Office Action, it is not a contact land for helping reduce problems associated with etch misalignments.

Further, it is acknowledged in the outstanding Official Action that the Watanabe reference does not disclose a second barrier layer with second source and drain contacts extending there through to establish communication with the source and drain contact lands. *See, Official Action* at page 2, ¶6. However, it is alleged therein that the Fukuda reference discloses such limitations and that it would have been obvious to one skilled in the art at the time of the invention to improve upon the device of the Watanabe reference in the manner of a more comprehensive interconnect structure as disclosed by the Fukuda reference for the purpose, for instance, of providing a multi-level interconnect structure that will provide greater device insulation of the device active region yet provide the desired conductivity of the Fukuda reference to upper level devices. *See id.* Applicant respectfully submits, however, that the Fukuda reference does not disclose a second barrier layer with second source and drain contacts extending there through to establish communication with the source and drain contact lands, as asserted.

Rather, the Fukuda reference discloses a memory cell structure, and method of making the same, in which a capacitor is formed in the uppermost layer of multiple, stacked metal wiring layers. *See, Fukuda reference* at col. 3, lines 48-56. In the memory cell structure of the Fukuda reference, a gate electrode 3 is formed in a first passivated insulating film layer 8, the gate electrode 3 spanning between diffusion layers 4 and 5 (*i.e.*, drain and source areas) on a silicon substrate 1. Contact plugs 9 are formed in the first passivated insulating film layer 8, one

connected to each diffusion layer 4, 5. *See id.* at col. 1, line 27; col. 3, lines 48-56. A second insulating film 12 is then formed over the first insulating film layer 8 and the contact plugs 9. A connecting pad 10 is subsequently formed in the second insulating film 12 over one of the contact plugs 9 (*i.e.*, the contact plug connected to one of the diffusion layers 4 or 5) and a bit line 10' is formed in the second insulating film 12 over another of the contact plugs 9 (*i.e.*, the contact plug 9 connected to the other of the diffusion layers 4 or 5). *See id.* at col. 6, lines 14-38; FIG. 1. A plug 14, *e.g.*, a tungsten plug, is subsequently formed in the second insulating film 12 over the connecting pad 10. *See id.* While in the memory cell structure of the Fukuda reference, the diffusion layers 4, 5 are not specifically denoted as source or drain regions, it is noted that the gate electrode 3 spans between a source region and a drain region, as known to those of ordinary skill in the art, and as recited in independent claim 3 of the present application.

In the memory cell structure of the Fukuda reference, a plug 14 is formed in the second insulating film 12 over ***only*** the connecting pad 10 and not over the bit line 10'. *See, Fukuda reference* at FIG. 1. Accordingly, the memory cell structure of the Fukuda reference discloses ***either*** an upper source contact extending through the second insulating film and in electrical communication with a source connecting pad ***or*** an upper drain contact extending through the second barrier layer and in electrical communication with a drain connecting pad ***but not both***. As such, it is respectfully submitted that the Fukuda reference fails to disclose a structure having each of the limitations of independent claim 3, as amended herein, which claim positively recites ***both*** an upper drain contact ***and*** an upper source contact. It is worth noting that while the memory cell structure of the Fukuda reference is disclosed to include more than one plug 14, it does not disclose an embodiment wherein the diffusion layers 4, 5 (*i.e.*, the source and drain areas) on either side of a gate electrode 3 both include upper contacts in communication therewith. *See, Fukuda reference* at FIG. 1.

In view of the above, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest each of the limitations of independent claim 3, as amended herein. As such, a *prima facie* case of obviousness of this claim cannot be established based upon the asserted combination of references. Accordingly, it is respectfully requested that

the rejection under 35 U.S.C. § 103(a) of claim 3 based upon the asserted combination of the Watanabe and Fukuda references be withdrawn.

Each of claims 4 through 6, 9 and 10 depend directly from claim 3 and, thus, a *prima facie* case of obviousness based upon the asserted combination of references also cannot be established for these claims. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) (dependent claims are nonobvious under 35 U.S.C. § 103(a) if the independent claims from which they depend are nonobvious). Thus, it is respectfully requested that the obviousness rejection of claims 4 through 6, 9 and 10 be withdrawn as well.

Independent claim 21 recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharges which includes similar structure to that recited in independent claim 3. Accordingly, Applicant submits that a *prima facie* case of obviousness based upon the combination of the Watanabe and Fukuda references cannot be established for claim 21 for at least the same reasons as those stated above with regard to claim 3. Additionally, each of claims 22 through 24, 27 and 28 depend directly from claim 21 and, thus, a *prima facie* case of obviousness based upon the asserted combination of references also cannot be established for these claims. *See, In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). Thus, it is respectfully requested that the obviousness rejection of claims 21 through 24, 27 and 28 be withdrawn as well.

Regarding claims 30 through 32, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference also fails to teach or suggest all of the limitations of these claims and, accordingly, a *prima facie* case of obviousness of these claims cannot be established based upon the asserted combination of references. With initial reference to independent claim 30, recited is a transistor for the dissipation of electrostatic discharges which comprises an intermediate structure. The intermediate structure comprises a substrate having at least one thick field oxide area and at least one active area. The at least one active area includes at least one implanted drain region and at least one implanted source region. The intermediate structure further includes at least one transistor gate member spanned between the at least one implanted drain region and the at least one implanted source region on the at least one active area. The

transistor further comprises a first barrier layer substantially covering the at least one thick field oxide area and the at least one active area, and adjacent the at least one transistor gate member. Still further, the transistor comprises a *second barrier layer* disposed over said first barrier layer *and planarized down to the at least one transistor gate member.* At least one drain contact plug and at least one source contact plug extend through *each of the first and second barrier layers*, the at least one drain contact plug being in electrical communication with the at least one drain region on the semiconductor substrate and the at least one source contact plug being in electrical communication with the at least one source region on said semiconductor substrate. Further, the transistor comprises an individual drain contact land disposed atop each of the at least one drain contact plugs and a portion of the second barrier layer, the individual drain contact land being wider than the at least one drain contact plug. An individual source contact land is disposed atop each of said at least one source contact plugs and a portion of said second barrier layer, the individual source contact land being wider than the at least one source contact plug. A *third barrier layer* is disposed over the second barrier layer, the individual drain contact land, and the individual source contact land. *At least one upper source contact extends through the third barrier layer, the at least one upper source contact being in electrical communication with the individual source contact land, and at least one upper drain contact extends through the third barrier layer, the at least one upper drain contact being in electrical communication with the individual drain contact land.*

It is respectfully submitted that neither the Watanabe reference nor the Fukuda reference teaches or suggests a structure having a first barrier layer and a second barrier layer, the second barrier layer planarized down to at least one transistor gate member. Rather, the Watanabe reference discloses a first barrier layer planarized down to a transistor gate member with a second barrier disposed thereover and the Fukuda reference fails to disclose a barrier layer planarized down to a transistor gate member at all. Further, as discussed above with regard to claim 3, neither the Watanabe reference nor the Fukuda reference teaches or suggests a structure having both an upper source contact and a upper drain contact extending through a barrier layer and in electrical communication with a source contact land and a drain contact land, respectively.

As such, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest each of the limitations of independent claim 30 and, thus, a *prima facie* case of obviousness cannot be established based upon this asserted combination of references. Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejection of claim 30 be withdrawn. Claim 30 is believed to be in condition for allowance and such favorable action is respectfully requested.

Independent claim 32 recites a semiconductor device including at least one transistor for the dissipation of electrostatic discharges which includes similar structure to that recited in independent claim 30. Accordingly, Applicant submits that a *prima facie* case of obviousness based upon the combination of the Watanabe and Fukuda references cannot be established for claim 32 for at least the same reasons as those stated above with regard to claim 30. Thus, it is respectfully requested that the obviousness rejection of claim 32 be withdrawn. Claim 32 is believed to be in condition for allowance and such favorable action is respectfully requested.

With regard to independent claim 31, a semiconductor device including at least one contact is recited. The semiconductor device comprises a single contact plug extending through *each of a first barrier layer and a second barrier, the second barrier layer disposed over the first barrier layer and planarized down to a transistor gate member.* The single contact plug is in electrical communication with an active region on a semiconductor substrate. The semiconductor device further includes an individual contact land disposed atop the single contact plug and a portion of the second barrier layer, the individual contact land being wider than the single contact plug. Still further, the semiconductor device comprises an upper contact extending through a third barrier layer, the third barrier layer disposed over the second barrier layer, to form and electrical contact with the individual contact land.

It is respectfully submitted that neither the Watanabe reference nor the Fukuda reference teaches or suggests a structure having a first barrier layer and a second barrier layer, the second barrier layer disposed over the first barrier layer and planarized down to at least one transistor gate member. Rather, as previously discussed, the Watanabe reference discloses a first barrier layer planarized down to a transistor gate member with a second barrier disposed thereover and

the Fukuda reference fails to disclose a barrier layer planarized down to a transistor gate member at all. Accordingly, it is respectfully submitted that the Watanabe reference in view of the Fukuda reference fails to teach or suggest each of the limitations of independent claim 31 and, thus, a *prima facie* case of obviousness cannot be established based upon this asserted combination of references. Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejection of claim 31 be withdrawn. Claim 31 is believed to be in condition for allowance and such favorable action is respectfully requested.

While there is no basis stated in the outstanding Official Action for the rejection of claim 29, it is stated in the Office Action Summary that such claim is rejected. It is worth noting that claim 29 includes similar structure to that recited in independent claim 31 and, accordingly, this claim is believed to be in condition for allowance over the asserted combination of references for at least the reasons stated with regard to claim 31.

CONCLUSION

Claims 3 through 6, 9, 10, 21 through 24 and 27 through 32 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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